Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1-30 (canceled)

1   Claim 31 (new): Apparatus for a bi-directional communication
2   link having a plurality of channels,
3   each of said channels comprising:
4   a master connected at a near end of the channel
5   and a slave connected at an opposite end of the channel, said
6   master comprising:
7   (a) a first transmitter coupled to the
8   channel and having a master Tx clock signal; and
9   (b) a first receiver coupled to the channel
10   and comprising:
11   (i) an analog-to-digital (A/D) converter
12   that periodically samples a signal incoming over the channel
13   to yield a received signal;
14   (ii) a clock recovery circuit that
15   generates a master Rx clock from a clock signal embedded in
16   the received signal; and
17   (iii) a metric processor, connected to
18   an output of said A/D converter, that produces a metric
19   signal reflective of amplitude differences between the
20   received signal and allowed amplitude levels for the received
21   signal; and
22   said slave comprising:

23   (a) a second receiver coupled to the channel

24 and comprising a clock recovery circuit for generating a

25 Slave Rx clock from a signal received over the channel and

26 transmitted from the master;

27   (b) a second transmitter coupled to the

28 channel and having a Slave Tx clock signal, said master Rx

29 clock signal being frequency locked to said Slave Tx clock

30 signal; and

31   (c) a first delay element for generating said

32 Slave Tx clock signal by controllably delaying said Slave Rx

33 clock signal; and

34   wherein said apparatus further comprises a decision

35 processor, connected to said master and responsive to said

36 metric signal, for determining a delay value to be provided

37 by said first delay element in the slave which will maximize

38 the metric signal and issuing a command, via the first

39 transmitter and the channel, to said second receiver in order

40 to set a delay provided by said first delay element to said

41 delay value, so as to reduce distortion caused by near end

42 cross-talk and echo in signals received over the channel, by

43 the first receiver and thus facilitate clock and data

44 recovery by the first receiver.

1   Claim 32 (new): The apparatus of claim 31 further comprising,

2 in the first receiver, a second delay element, situated

3 between said Master Rx clock signal and said A/D converter

4 and responsive to said decision processor, which controllably

5 delays a sampling time, Ts, provided by said converter,

6 wherein said decision processor independently sets the delays

7 provided by the first and second delay elements in order to

8 further maximize the metric signal.

1   Claim 33 (new): The apparatus of claim 32 wherein the metric
2   processor comprises a processor for computing a proportion of
3   samples of the received signal provided by the master falling
4   within the allowed amplitude levels relative to those of said
5   samples that fall outside of the allowed amplitude levels.

1   Claim 34 (new): The apparatus of claim 33 wherein said
2   decision processor is connected to all the masters and is
3   responsive to the metric signal produced in each of the
4   masters so as to change the phase in each corresponding one
5   of the slaves in order to maximize all the metric signals
6   produced by all the masters.

1   Claim 35 (new): The apparatus of claim 31 wherein said
2   decision processor is connected to all the masters and is
3   responsive to the metric signal produced in each of the
4   masters so as to change the phase in each corresponding one
5   of the slaves in order to maximize all the metric signals
6   produced by all the masters.

1   Claim 36 (new): The apparatus of claim 31 wherein the metric
2   processor comprises a processor for computing a proportion of
3   samples of the received signal provided by the master falling
4   within the allowed amplitude levels relative to those of said
5   samples that fall outside of the allowed amplitude levels.

1   Claim 37 (new): The apparatus of claim 36 wherein said
2   decision processor is connected to all the masters and is
3   responsive to the metric signal produced in each of the
4   masters so as to change the phase in each corresponding one
5   of the slaves in order to maximize all the metric signals
6   produced by all the masters.

1   Claim 38 (new): Apparatus for a bi-directional communication
2   link having a plurality of channels with a master and a slave
3   at respective ends of each one of the channels so as to
4   define respective pluralities of masters and slaves, the
5   master issuing a Master Tx clock, the slave constructing both
6   a Slave Rx clock frequency-locked to the Master Tx clock and
7   a Slave Tx clock frequency-locked to the Slave Rx clock, said
8   apparatus comprising:
9   a metric processor, situated within said master, which
10   produces a metric signal reflective of amplitude differences
11   between a signal received by the master from a corresponding
12   one of the slaves and allowed amplitude levels of the
13   received signal; and
14   a decision processor, connected to the master and
15   responsive to the metric processor, for changing phase of the
16   Slave Tx clock relative to the Slave Rx clock in the
17   corresponding one of the slaves in order to maximize the
18   metric signal produced by the metric processor and thereby
19   reduce distortion caused by near end cross-talk and echo in
20   signals received over the channel by a receiver in the master
21   and thus facilitate clock and data recovery by the receiver.

1   Claim 39 (new): The apparatus of claim 38 wherein said metric
2   processor comprises a processor for computing a proportion of
3   samples of the received signal provided by each of said
4   masters and which fall within the allowed amplitude levels
5   relative to those ones of said samples that fall outside of
6   the allowed amplitude levels.

1   Claim 40 (new): The apparatus of claim 34 wherein said
2   decision processor is connected to all the masters and is
3   responsive to the metric signal produced in each of the

4 masters so as to change the phase in each corresponding one

5 of the slaves in order to maximize all the metric signals

6 produced by all the masters.

1 Claim 41 (new): The apparatus of claim 38 wherein said

2 decision processor is connected to all the masters and is

3 responsive to the metric signal produced in each of the

4 masters so as to change the phase in each corresponding one

5 of the slaves in order to maximize all the metric signals

6 produced by all the masters.